

ABSTRACT

A power-on reset circuit comprises a power supply voltage detection circuit that detects a rise of a power supply voltage and that changes a logic level of a first internal node; a capacitor charge/discharge circuit that charges and discharges a capacitor according to the first internal node level and that in an event that the power supply voltage is reduced, discharges the capacitor to follow the event; and a reset pulse generation circuit that before the power supply voltage rises higher than the predetermined voltage, outputs a first output voltage to an output node and that after the power supply voltage has risen higher than the predetermined voltage, outputs a second output voltage to the output node upon detecting that a charge level of the capacitor has become higher than a charge level detection voltage.

Reference: FIG. 1